IN THE CLAIMS

We claim:

1. A semiconductor device comprising:

an electrode having a first thickness;

a silicide layer on said electrode, said silicide layer having a second thickness; and

a sidewall spacer adjacent to said electrode, wherein said sidewall spacer has a height greater than the sum of said first thickness and said second thickness.

2. A metal oxide semiconductor device comprising:

a gate electrode having a first thickness;

a silicide layer on said gate electrode, said silicide layer having a second thickness;

a pair of sidewall spacers on opposite sides of said gate electrode, said sidewall spacers having a height which is greater than the sum of said first thickness and said second thickness; and

a pair of source/drain regions formed on opposite sides of said gate electrode.

3. The semiconductor device of claim 2 wherein said gate electrode comprises polysilicon.

4. The semiconductor device of claim 2 wherein said gate electrode further comprises selectively deposited semiconductor on said polysilicon layer.

5. A semiconductor device comprising:

a gate electrode formed on a gate dielectric layer formed on a first surface of a substrate;

a pair of source/drain regions formed on opposite sides of said gate electrode;

an isolation region having a top surface extending less than 1500Å above said first substrate surface; and

a silicide layer formed on said source/drain regions wherein said silicide layer has a top surface with a height less than said top surface of said isolation region.

6. The semiconductor device of claim 5 further comprising:

a gate silicide layer having a first thickness formed on said gate electrode, said gate electrode having a second thickness; and

a pair of sidewall spacers formed on opposite sides of said gate electrode, wherein said sidewall spacers have a height which is greater than the sum of said first thickness and said second thickness.

7. A method of forming a semiconductor device comprising the steps of:

forming an electrode having a first thickness;

forming a silicide layer having a second thickness on said electrode; and

forming a sidewall spacer adjacent to said gate electrode wherein said sidewall spacer has a height which is greater than the sum of said first thickness and said second thickness.

8. A method of forming an MOS transistor comprising the steps of:

forming a gate electrode on a gate dielectric layer formed on a first surface of a substrate;

forming a pair of source/drain regions on opposite sides of said gate electrode;

forming an isolation region having a top surface extending less than 1500Å above said first substrate surface; and

forming a silicide layer on said pair of source/drain regions wherein said silicide layer has a top surface with a height less than the top surface of said isolation region.

9. The method of claim 8 further comprising the steps of:

forming a gate silicide layer having a first thickness on said gate electrode, wherein said gate electrode has a second thickness; and

forming a pair of sidewall spacers on opposite sides of said gate electrode, wherein said sidewall spacers have a height which is greater than the sum of said first thickness and said second thickness.

10. A method of forming a semiconductor device, said method comprising the steps of:

forming a gate dielectric layer on a silicon substrate;

forming a silicon layer over said gate dielectric layer said silicon layer having a first thickness;

forming a sacrificial layer over said silicon layer;

patterning said silicon layer and said sacrificial layer into an electrode;

forming a pair of spacers on opposite sides of said electrode said spacers having a first height;

removing said sacrificial layer from over said silicon layer; and

forming a silicide having a second thickness on said silicon layer and on said substrate adjacent to the outside edges of said spacers, wherein said first height is greater than the sum of said first thickness and said second thickness.

11. The method of claim 10 wherein said sacrificial layer is silicon germanium.

12. The method of claim 10 wherein said spacers comprise silicon nitride.

13. The method of claim 10 wherein said sacrificial layer comprises silicon dioxide.

14. The method of claim 13 wherein said silicon dioxide layer is doped with fluorine.

15. The method of claim 10 wherein said sacrificial layer is removed with a wet etchant.

16. The method of claim 10 further comprising the step of:

polishing said silicon layer prior to forming said sacrificial layer.

17. The method of claim 10 further comprising the step of:

doping said silicon layer after removing said sacrificial layer.

18. The method of claim 10 wherein said step of forming said silicide layer comprises the steps of:

blanket depositing a refractory metal over said substrate, said pair of sidewall spacers, and said silicon layer;

thermally reacting said refractory metal with said substrate and said silicon layer to form a refractory metal silicide; and

removing said refractory metal from said pair of spacers.

19. The method of claim 10 wherein said step of forming said silicide layer comprises the step of:

selectively depositing said silicide layer on said silicon layer and on said substrate.

20. The method of claim 10 wherein said spacers have a height greater than the sum of the thickness of said silicon layer and said silicide layer.

21. The method of claim 10 wherein said silicon layer is polycrystalline silicon.

22. The method of claim 10 wherein said spacer height is greater than the sum of said silicon thickness plus said gate dielectric thickness.

23. A method of forming a device, said method comprising the steps of:

forming a silicon electrode having a first thickness;

forming a metal layer on said silicon electrode; and

forming a silicide on said silicon electrode by reacting said metal layer and said silicon gate electrode, wherein said silicide has a second thickness, said second thickness at least twice said first thickness.

24. A method of forming a semiconductor device in a semiconductor substrate comprising the steps of:

forming an isolation region in said semiconductor substrate;

etching said semiconductor substrate adjacent to said isolation region to form a recess region; and

forming a silicide in said recessed region.

25. A method of forming an integrated circuit comprising the steps of:

forming an isolation region in a semiconductor substrate, said isolation region having a top surface extending less than 1500Å above said semiconductor substrate;

forming a first and second diffusion region adjacent to and on opposite sides of said isolation region in said semiconductor substrate; and

forming silicide on said first and second diffusion regions wherein said silicide has a top surface with a height less than the top surface of said isolation region.

26. A method of forming a semiconductor device, said method comprising the steps of:

forming a silicon film above a substrate;

forming a silicon germanium film on said silicon film;

patterning said silicon film and said silicon germanium film into an intermediate electrode;

forming a pair of sidewall spacers on opposite sides of said intermediate electrode;

removing said silicon germanium film from said intermediate electrode to reveal said silicon film; and

forming a silicide film on said silicon film.

27. The method of claim 26 wherein said silicon film is polycrystalline silicon.

28. The method of claim 26 wherein said silicon germanium film is removed with a mixture of NH_4OH and H_2O_2.

29. The method of claim 26 wherein said silicon germanium film is removed with sulfuric acid (H_2SO_4).